



Appl. No. 09/735,267  
Amdt. dated August 10, 2004

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Original) A computer system, comprising:
  - a first computer bus connected to a first plurality of bus devices;
  - a second computer bus connected to a second plurality of bus devices;
  - a bridge coupling together said first computer bus and said second computer bus;
  - a first multicast bus connecting to said first plurality of bus devices and a second multicast bus connecting to said second plurality of bus devices;wherein one of the first plurality of bus devices is capable of transmitting a multicast signal to at least two of said second plurality of bus devices, which are identified by a signal transmitted on said first multicast bus and said second multicast bus.
2. (Original) The system of claim 1, wherein the first plurality of bus devices are capable of transmitting a sideband signal to said bridge indicating a multicast cycle.
3. (Original) The system of claim 2, wherein the bridge relays the multicast cycle to said second computer bus in response to receipt of the sideband signal.
4. (Original) The system of claim 3, wherein said at least two of said secondary plurality of bus devices that are identified by a signal transmitted on the first and second multicast busses, each receive and decode the multicast cycle relayed by said bridge.

1 5. The system of claim 4, wherein said bridge also transmits a sideband signal to said second  
2 plurality of bus devices substantially simultaneously with relaying the multicast cycle.

1 6. The system of claim 5, wherein said first computer bus and said second computer bus  
2 comprise a PCI bus and said bridge comprises a PCI-to-PCI bridge.

1 7. The system of claim 2, wherein said bridge comprises a PCI-to-host bridge that connects to  
2 a host bus.

1 8. The system of claim 7, wherein said second computer bus comprises a second PCI bus, and  
2 a second PCI-to-host bridge couples said host bus to said second PCI bus.

1 9. The system of claim 8, wherein the first PCI-to-host bridge transmits a sideband signal to  
2 said second PCI-to-host bridge indicating a multicast cycle originating on said first PCI bus.

1 10. The system of claim 9, wherein in response to the sideband signal from said first PCI-to-  
2 host bridge, said second PCI-to-host bridge captures data transmitted on said host bus from said  
3 first PCI-to-host bridge.

1 11. The system of claim 10, wherein the second PCI-to-host bridge relays the data captured  
2 from the host bus onto the second PCI bus, and wherein said at least two of said secondary  
3 plurality of bus devices that are identified by a signal transmitted on the first and second multicast  
4 busses, each receive and decode the multicast cycle relayed by said second PCI-to-host bridge.



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12. (Original) The system of claim 11, wherein said second PCI-to-host bridge also transmits a sideband signal to said second plurality of bus devices substantially simultaneously with relaying the multicast cycle.

13. (Original) The system of claim 1, wherein one of the second plurality of bus devices is capable of transmitting a multicast signal to at least two of said first plurality of bus devices, which are identified by a signal transmitted on said first and second multicast busses.

14. (Original) The system of claim 3, wherein the sideband signals are transmitted on the multicast busses.

15. (Original) The system of claim 12, wherein the sideband signals are transmitted on the multicast busses.

16. (Original) A method of transmitting a multicast signal between a device on a first bus to multiple targets on a second bus, and wherein the first bus and the second bus are coupled together by at least one bus bridge, comprising the acts of:

- generating data on the first bus that is intended for multiple targets on the second bus;
- identifying the multiple targets on the second bus via a target identification signal transmitted on a first and second multicast bus; and
- signaling the bridge that a multicast cycle has been initiated on the first bus;
- relaying the data on the first bus to the second bus by the bridge;
- indicating that data for a multicast cycle is appearing on the second bus;
- and
- capturing the multicast data at the targets identified by the target identification signal.



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17. (Original) The method of claim 16, wherein the act of generating data on the first bus includes transmitting data on the first bus according to the protocol of the first bus.
18. (Original) The method of claim 16, wherein the act of signaling the bridge occurs via a sideband signal between the device generating the data and the bridge.
19. (Original) The method of claim 16, wherein the act of indicating the data for a multicast cycle is appearing on the second bridge occurs via a sideband signal between the bridge and devices resident on the second bus.
20. (Currently amended) The method system of claim 16, wherein the first bus and the second bus comprise PCI busses.
21. (Currently amended) The method system of claim 20, wherein the bridge comprises a PCI-to-PCI bridge.
22. (Currently amended) The method system of claim 20, wherein two bridges couple the PCI busses together.
23. (Currently amended) The method system of claim 22, wherein the two bridges are connected to a host bus.
24. (Currently amended) The method system of claim 23, wherein the two bridges comprise PCI-to-host bridges.